

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Rev 1.0: Release to market

Rev 1.1: Update DEVICE ORDER INFORMATION

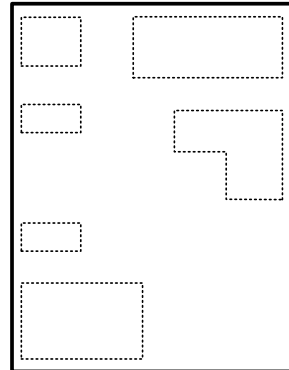
Rev 1.2: Update Recommended Component Selections and Recommended FB Resistor Range

Rev 1.3: Update Output Voltage Range and TAPE AND REEL INFORMATION

SCT2233MLUAR	Tape & Reel	5000	7	7L ECLGA (2.5mmX1.7mm)	3
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Over operating free-air temperature unless otherwise noted⁽¹⁾

V_{IN}	-0.3 to 19	V
V_{SW}	-1 to 19	V
$V_{SW} < 10ns$	-2.5 to 21	V
V_{BST}	$V_{SW}-0.3$ to $V_{SW}+6$	V
V_{FB}	-0.3 to 6.5	V
V_{EN}	-0.3 to 6.5	



SCT2233M Top View
(2.5mm x 1.7mm)

VOUT	1	Power output, please use as large an output capacitor as possible to reduce output voltage ripple.
FB	2	Buck converter output feedback sensing voltage. Connect a resistor divider from VOUT to FB to set up output voltage. The device regulates FB to the internal reference of 0.8V typical.
EN	3	Enable logic input. The device has precision enable thresholds 1.2V rising / 1.12V falling for programmable UVLO threshold and hysteresis.
BST	4	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1µF or greater ceramic capacitor between BST pin and SW node.
SW	5	Power Switching Output. SW is the switching node that supplies power to the output. Note that a capacitor is required from SW to BST to power the high-side switch.
VIN	6	Power supply input. VIN supplies the power to the IC, as well as the step-down converter switches. Drive VIN with a 4.2V to 8.5V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See Input Capacitor.
PGND	7	Power ground. Must be soldered directly to ground plane.

Over operating free-air temperature range unless otherwise noted

V _{IN}	Input voltage range	4.2	8.5	V
T _J	Operating junction temperature	-40	125	°C

V _{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins ⁽¹⁾	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins ⁽¹⁾	-0.5	+0.5	kV

$V_{IN}=8.5V$, $T_J=-40\text{ }^{\circ}\text{C}\sim 125\text{ }^{\circ}\text{C}$, typical values are tested under $25\text{ }^{\circ}\text{C}$.

V_{IN}	Operating input voltage		4.2	8.5	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising	4.0		V
			350		mV
I_{SD}	Shutdown current	EN=0, No load, $V_{IN}=8.5V$	0.9		μA
I_Q	Quiescent current	EN=2V, No load, No switching. $V_{IN}=8.5V$. BST-SW=5V	205		μA
V_{EN_H}	Enable high threshold		1.2		V
V_{EN_L}	Enable low threshold		1.12		V
R_{DSON_H}	High side FET on-resistance		50		m
R_{DSON_L}	Low side FET on-resistance		24		m
V_{FB}	Feedback Voltage	$T_J=25\text{ }^{\circ}\text{C}$, CCM	0.788	0.8	0.812
					V
I_{LIM_LSD}	LSD valley current limit		2.4	3.2	4
					A
F_{SW}	Switching frequency	$V_{IN}=8.5V$, $V_{OUT}=5V$	1200		kHz
$t_{ON_MIN}^*$	Minimum on-time		70		ns
t_{OFF_MIN}	Minimum off-time		220		ns
t_{SS}	Internal soft-start time		3		ms
T_{SD}^*	Thermal shutdown threshold Hysteresis	T_J rising	155		$^{\circ}\text{C}$
			25		

Figure 1. Efficiency vs Load Current (VIN=7.2V)

Figure 2

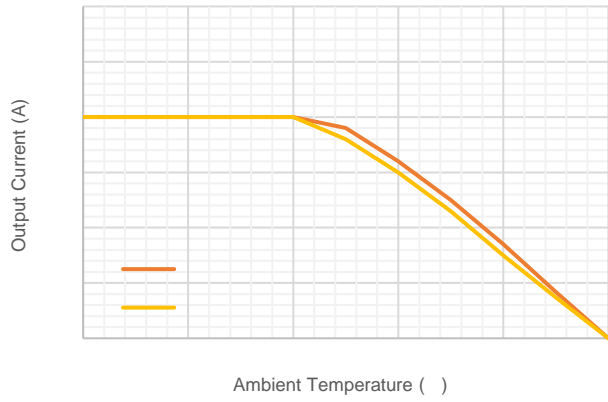


Figure 7. Thermal Derating (VOUT=1.8V, $J_A=60\text{ }^\circ\text{C/W}$)

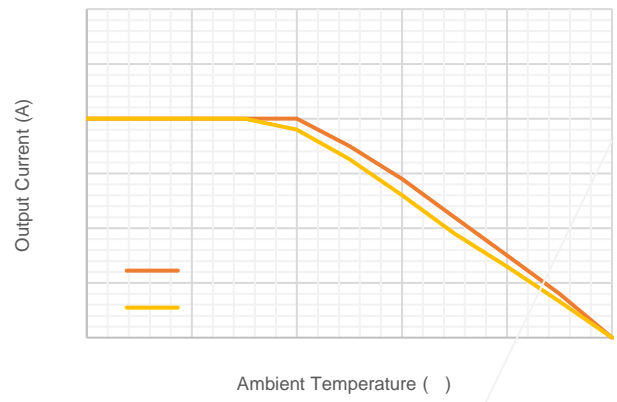


Figure 8. Thermal Derating (VOUT=3.3V, $J_A=60\text{ }^\circ\text{C/W}$)

Figure 9. Thermal Derating (VOUT=5V, $J_A=60\text{ }^\circ\text{C/W}$)

The SCT2233M device is 4.2-8.5V input, 2A output, synchronous step-down converter module with internal power MOSFETs. Adaptive constant on-time (ACOT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET is turned on for a fixed one shot time ON-time period. The one shot time is calculated by the converter's input voltage (VIN) and the output voltage (VOUT) cycle-by-cycle based to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. SCT2233M turns off high-side MOSFET after the fixed on time and turns on the low-side MOSFET. SCT2233M turns off the low-side MOSFET once the output voltage dropped below the output regulation, the one-shot timer then reset and the high-side MOSFET is turned on again. The on-time is inversely proportional to the input voltage and proportional to the output voltage. It can be calculated using the following equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

Where:

- VOUT is the output voltage.
- VIN is the input voltage.
- fs is the switching frequency.

After an ON-time period, the regulator goes into the OFF-time period. The OFF-time period length depends on VFB in most cases. It will end when the FB voltage decreases below 0.8V, at which point the ON-time period is triggered. If the OFF-time period is less than the minimum OFF time, the minimum OFF time will be applied, which is around 220ns typical.

The SCT2233M is designed with Power Save Mode (PSM) at light load conditions for high



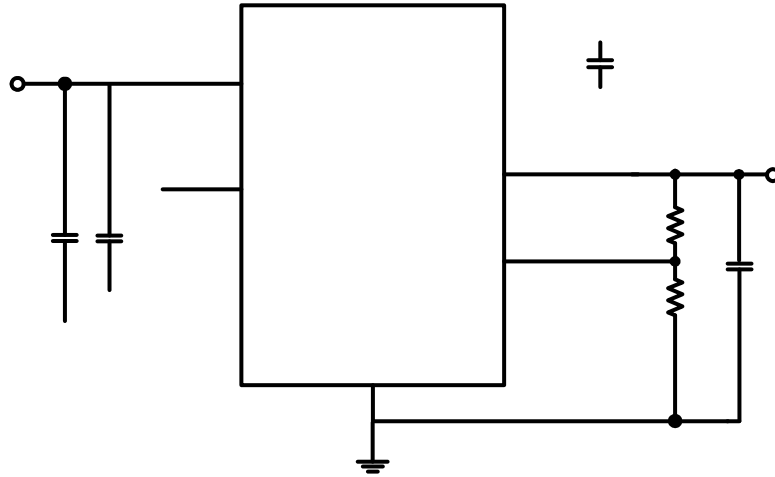


Figure 12. 8.5V Input, 3.3V/2A Output

Input Voltage	8.5V
Output Voltage	3.3V
Output Current	2A
Switching Frequency	1.2MHz
Output voltage ripple (peak to peak)	25mV
Transient Response 0.5A to 1.5A load step	Vout = 120mV



Vin=8.5

The maximum IC junction temperature should be restricted to 125 °C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation (9).

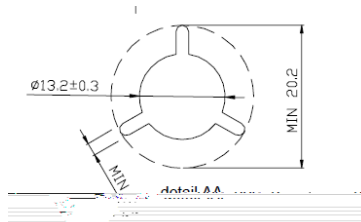
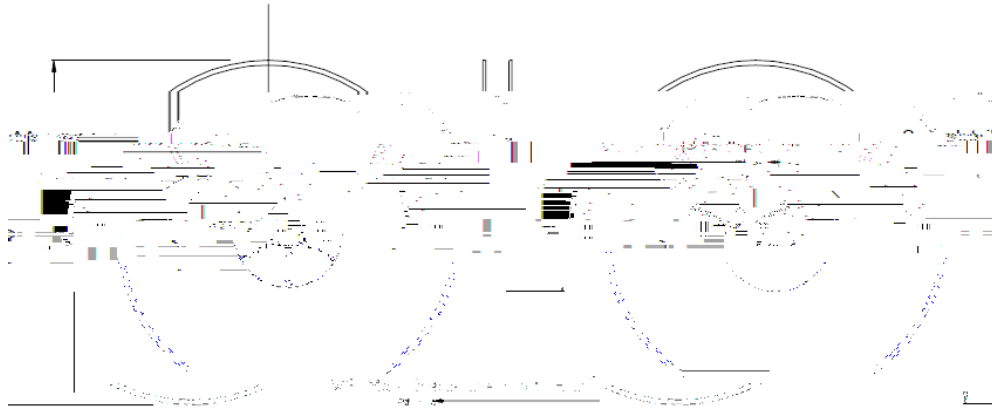
$$\text{—————} \tag{7}$$

where

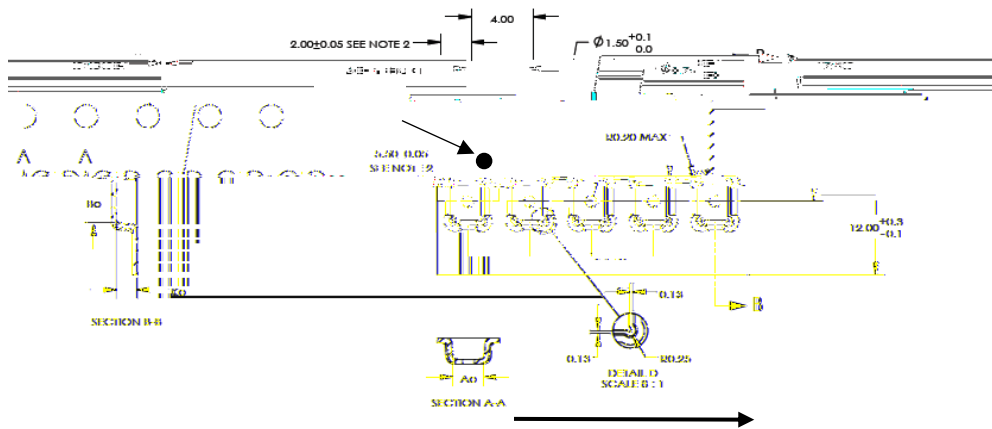
T_A is the maximum ambient temperature for the application.

R_{JA} is the junction-to-ambient thermal resistance.

The real junction-to-ambient thermal resistance R_{JA} of the package greatly depends on the PCB type, layout, thermal pad connection and environmental factor. Using thick PCB copper and soldering the GND t(r)-3((n14c4.63n)39(gt)-10(h



	176	178	330
	58	60	62
	124	-	-
	-	-	144
TYPE WIDTH	-	12.00	-



	1.90	2.00	2.10
	2.70	2.80	2.90
	1.3	1.35	1.45