3.8V-36V Vin, 3A Synchronous Step-down DCDC Converter

FEATURES

- EMI Reduction with Switching Node Ringing-free
- 400kHz Switching Frequency with 6% Frequency Spread Spectrum (FSS)
- Pulse Skipping Mode PSM in Light Load Condition
- 3.8V-36V Wide Input Voltage Range
- Up to 3A Continuous Output Load Current
- 0.8V ±1% Feedback Reference Voltage
- Fully Integrated 80mΩ R_{dson} High Side MOSFET and 42mΩ R_{dson} Low Side MOSFET
- 1uA Shut-down Current
- 80ns Minimum On-time
- Precision Enable Threshold for Programmable UVLO Threshold and Hysteresis
- Low Drop out (LDO) Mode Operation
- 4ms Built-in Soft Start Time
- Output Over Voltage Protection
- Thermal Shutdown Protection at 160°C
- Available in TSOT23-6L Package

APPLICATIONS

- General Consumer
- Industrial Control System
- Automotive System

DESCRIPTION

The SCT9430 is 3A synchronous buck converters with up to 3

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Release to Market.

Revision 1.1: Update DEVICE ORDER INFORMATION.

DEVICE ORDER INFORMATION

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SCT9430TVBR	Tape & Reel	3000	9430	6	TSOT23-6

ABSOLUTE MAXIMUM RATINGS

Over operating free-

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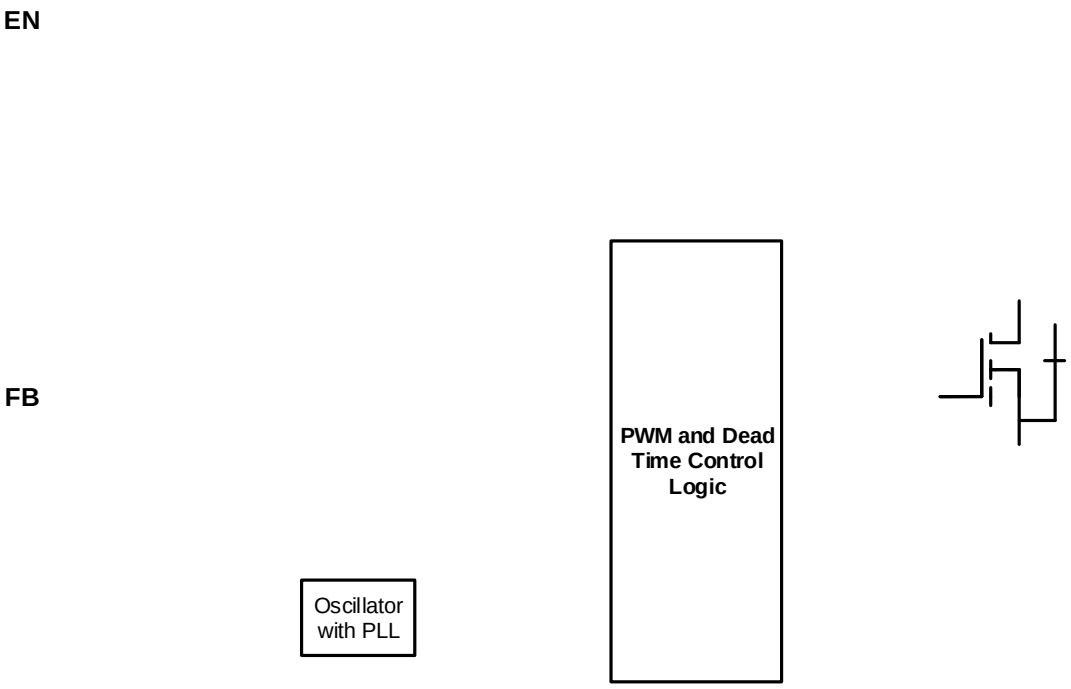
TYPICAL CHARACTERISTICS

Figure 1. Efficiency vs Load Current, Vin=12V

Figure 2. Efficiency vs Load Current, Vin=24V

Figure 3

FUNCTIONAL BLOCK DIAGRAM



operation is disabled when EN voltage falls below its lower threshold (typically 1.1V/fall).

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In buck converter, the switching node ringing amplitude and cycles are critical especially related to the high frequency radiation EMI noise. The SCT9430 implements the multi-level gate driver speed technique to achieve the switching node ringing-free without scarifying the switching node rise/fall slew rate and power efficiency of the converter. The switching node ringing amplitude and cycles are damped by the built-in MOSFETs gate driving technique (SCT Patented Proprietary Design). The switching node zoomed in wave form is shown in Figure 9.

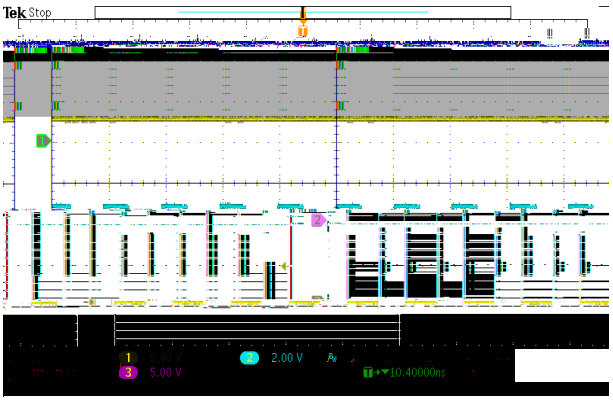

Figure 9. SCT9430 Switching Node Waveform

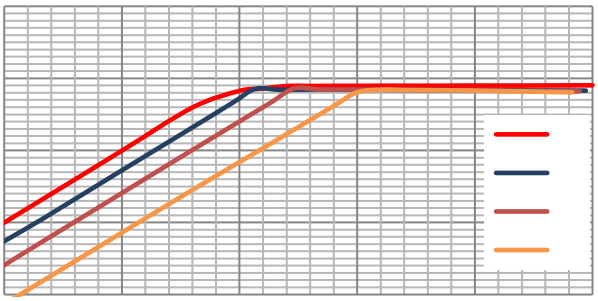

Figure 10. SCT9430 LDO Mode Waveform

The SCT9430 has cycle-by-cycle peak current limit with sensing the internal high side MOSFET Q1 current during overcurrent condition. While the Q1 turns on, its conduction current is monitored by the internal sensing circuitry. Once the high-side MOSFET Q1 current exceeds the limit, it turns off immediately. If the Q1 over current time exceeds 512 switching cycles (hiccup waiting time), the buck converter enters hiccup mode and shuts down. After 8192 cycles off, the buck converter restarts to power up. The hiccup modes reduce the power dissipation in over current condition.

Both SCT9430 features buck converter output over voltage protection (OVP). If the output feedback pin voltage exceeds110% of feedback reference voltage (0.8V), the converter stops switching immediately. When the output feedback pin voltage drops below 105% of feedback reference voltage, the converter resumes to switching. The OVP function prevents the connected output circuitry damaged from un-predictive overvoltage. Featured feedback overvoltage protection also prevents dynamic voltage spike to damage the circuitry at load during fast loading transient.

The high-side MOSFET Q1 has minimum on-time 80ns typical limitation. While the device operates at minimum on-time, further increasing VIN results in pushing output voltage beyond regulation point. With output feedback over voltage protection, the converter skips pulse by turning off high-side MOSFET Q1 and prevents output running away higher to damage the load.

In heavy load condition, the SCT9430 forces the device operating at forced Pulse Width Modulation (PWM) mode. When the load current decreasing, the internal COMP net voltage decreases as the inductor current down. With the load current further decreasing, the COMP net voltage decreases and be clamped at a voltage corresponding to the 600mA peak inductor current. When the load current approaches zero, the SCT9430 enter Pulse Skipping Mode (PSM) mode to increase the converter power efficiency at light load condition. When the inductor current decreases to zero, zero-cross detection circuitry on high-side MOSFET Q1 forces the Q1 off till the beginning of the next switching cycle. The buck converter does not sink current from the load when the output load is light and converter works in PSM mode.

An external bootstrap capacitor between BST and SW pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

The floating supply (BST to SW) UVLO threshold is 2.7V rising and hysteresis of 350mV. When the converter operates with high duty cycle or prolongs in sleep mode for certain long time, the required time interval to recharging bootstrap capacitor is too long to keep the voltage at bootstrap capacitor sufficient. When the voltage across bootstrap capacitor drops below 2.35V, BST UVLO occurs. The SCT9430 intervenes to turn on low side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee operation over a wide duty range.

To support the application of small voltage-difference between Vout and Vin, the Low Drop Out (LDO) Operation is implemented by the SCT9430. The Low Drop Out Operation is triggered automatic when the off time of the high-side power MOSFET exceeds the minimum off time limitation.

In low drop out operation, high-side MOSFET remains ON as long as the BST pin to SW pin voltage is higher than BST UVLO threshold. When the voltage from BST to SW drops below 2.35V, the high-side MOSFET turns off and low-side MOSFET turns on to recharge bootstrap capacitor periodically in the following several switching cycles. Only 100ns of low side MOSFET turning on in each refresh cycle minimizes the output voltage ripple. Low-side MOSFET may turn on for several times till bootstrap voltage is charged to higher than 2.7V for high-side

MOSFET working normally. Then high-side MOSFET turns on and remains on until bootstrap voltage drops to trigger bootstrap UVLO again. Thus, the effective duty cycle of the switching regulator during Low Drop-out LDO operation can be very high even approaching 100% as shown in Figure 10.

During ultra-low voltage difference of input and output voltages, i.e. the input voltage ramping down to power down, the output can track input closely thanks to LDO operation mode.

Once the junction temperature in the SCT9430 exceeds 160°C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 125°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

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APPLICATION INFORMATION

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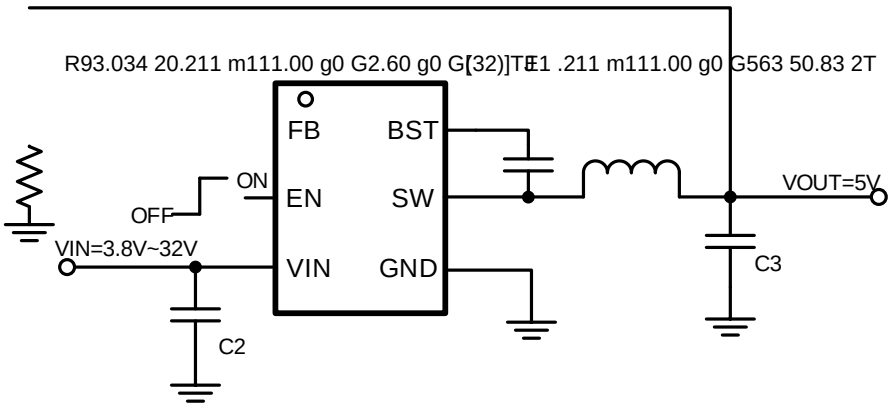

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Design Parameters	Example Value
Input Voltage	24V
Output Voltage	5V
Output Current	3A
Output voltage ripple (peak to peak)	±0.3V
Switching Frequency	400kHz

loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss.

F For buck converter, the output capacitor value determines the regulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

For small output voltage ripple, tsebl lu .

The SCT9430 has the internal integrated loop compensation as shown in the function block diagram. The compensation network includes a 18k resistor and a 7.6nF capacitor. Usually, the type II compensation network has a phase margin between 60 and 90 degrees. However, if the output capacitor has ultra-low ESR, the converter

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Vin=24V, Vout=5V, unless otherwise noted

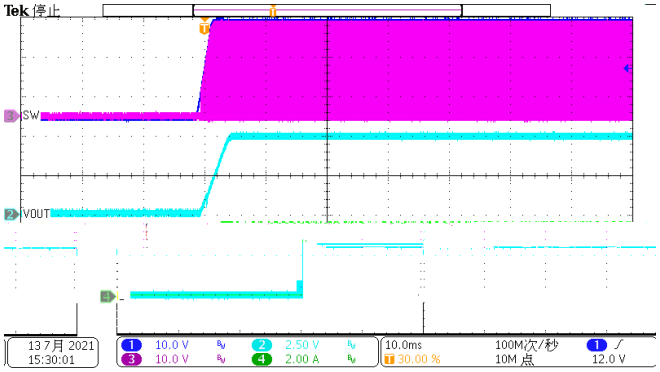

Figure 8. Power up(Iload=3A)

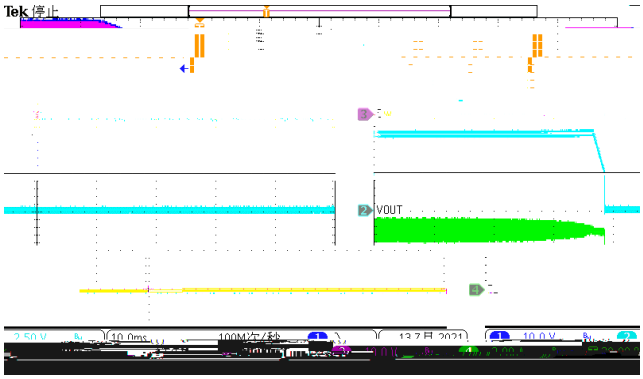

Figure 9. Power down(Iload=3A)

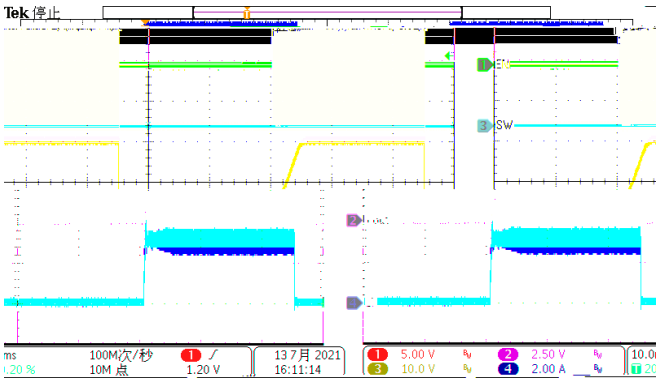

Figure 10.EN toggle (Iload=3A)

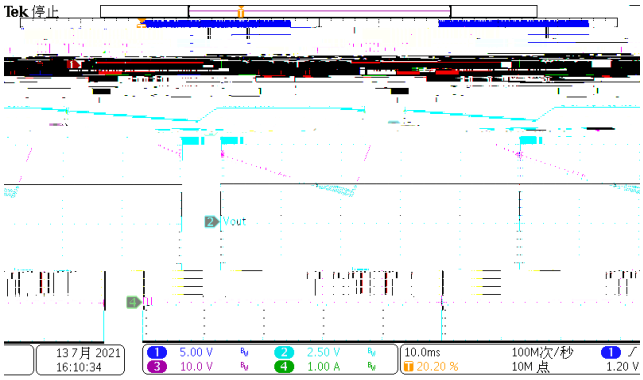

Figure 15. EN toggle (Iload=10mA)

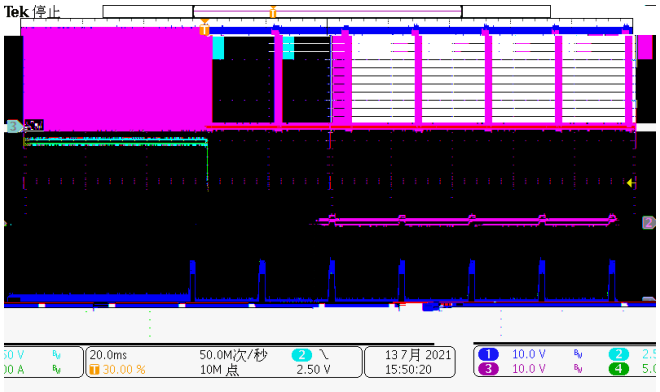

Figure 16. Over Current Protection(0.1A to hard short)

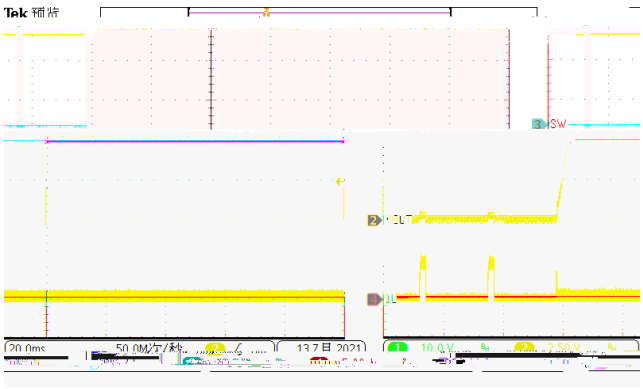

Figure 17. Over Current Release (hard short to 0.1A)

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Vin=24V, Vout=5V, unless otherwise noted

The regulator could suffer from instability and noise problems without carefully layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be very close to the VIN pin and GND pin to reduce the input supply ripple. Place the capacitor as close to VIN pin as possible to reduce high frequency ringing voltage on SW pin as well. Figure 24 is the recommended PCB layout of SCT9430.

The layout needs be done with well consideration of the thermal. A large top layer ground plate using multiple thermal vias is used to impr la[m] eel-ę -tiaẅ [T] -diatma obe

TAPE AND REEL INFORMATION